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IN THE CLAIMS

**Claim 1 (currently amended): A method of forming [[and]] an FET device with a raised silicon source/drain and a gate electrode structure on an SOI structure comprising an [[SOI]] silicon layer formed on a substrate wherein the substrate comprises an insulator by the following steps:**

forming a SiGe layer over the silicon layer,

forming a raised source/drain layer over the SiGe layer,

etching through the raised source/drain layer and the SiGe layer to form a gate electrode space with walls reaching down through the raised source/drain layer and the SiGe layer to the surface of the silicon layer thereby forming a pair of raised source/drain regions separated by the gate electrode space in the source/drain layer,

lining the walls of the gate electrode space with an internal etch stop layer and [[an]] inner sidewall spacers,

forming a gate electrode inside the inner sidewall spacers on a cleaned surface of the silicon layer,

forming external sidewall spacers adjacent to the gate electrode between the raised source/drain regions adjacent to the inner sidewall spacers, and

doping the source/drain regions. [[,]]

whereby a recessed channel is formed in the SOI silicon layer between the raised source/drain regions thereabove [[above]] and below the level of the SiGe layer.

**Claim 2 (original): The method of claim 1 wherein an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space.**

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**Claim 3 (original):** The method of claim 1 including the steps of forming the gate electrode space by the steps as follows:

- forming a dummy gate over the source/drain layer,
- forming a conformal outside spacer layer over the dummy gate,
- forming an exterior masking layer over the outside spacer layer,
- etching back the exterior masking layer to expose the dummy gate, and
- removing the dummy gate to form the gate electrode space.

**Claim 4 (original):** The method of claim 3 wherein the exterior masking layer is composed of silicon dioxide which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof.

**Claim 5 (currently amended):** The method of claim 3 wherein:

- an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space, and
- the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer.

**Claim 6 (original):** The method of claim 2 including the steps of forming the gate electrode space by the steps as follows:

- forming a dummy gate over the source/drain layer,
- forming a conformal outside spacer layer over the dummy gate,
- forming an exterior masking layer over the outside spacer layer,
- etching back the exterior masking layer to expose the dummy gate, and
- removing the dummy gate to form the gate electrode space.

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**Claim 7 (currently amended):** The method of claim 1 wherein:

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space; [[and]]

forming the gate electrode space by forming a dummy gate over the source/drain layer,

forming a conformal outside spacer layer composed of SiGe over the dummy gate,

forming an exterior masking layer over the outside spacer layer composed of silicon nitride,

etching back the exterior masking layer to expose the dummy gate, and

removing the dummy gate to form the gate electrode space.

**Claim 8 (original):** The method of claim 1 wherein the insulator forming the substrate comprises silicon oxide.

**Claim 9 (currently amended):** The method of claim 3 wherein:

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space, and

the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer.

**Claim 10 (currently amended):** The method of claim 3 wherein:

an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space,

the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer, [[and]]

performing a raised source extension region and a raised drain extension region implant, and

then forming an exterior spacer aside from the gate electrode.

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**Claim 11 (currently amended): A method of forming an FET device with a raised silicon source/drain and a gate electrode structure on an SOI structure comprising an [[SOI]] silicon layer formed on a substrate wherein the substrate comprises an insulator by the following steps:**

- forming a SiGe layer over the silicon layer,**
- forming a raised source/drain layer over the SiGe layer,**
- forming an etch stop layer over the raised source/drain layer,**
- forming a dummy gate over the source/drain layer,**
- forming a conformal outside spacer layer over the dummy gate,**
- forming an exterior masking layer over the outside spacer layer,**
- etching back the exterior masking layer to expose the dummy gate,**
- removing the dummy gate to form [[the]] a gate electrode space,**
- etching through the raised source/drain layer and the SiGe layer to form a gate electrode space with walls reaching down through the raised source/drain layer and the SiGe layer to the surface of the silicon layer thereby forming a pair of raised source/drain regions separated by the gate electrode space in the source/drain layer,**
- lining the walls of the gate electrode space with an internal etch stop layer and [[an]] inner sidewall spacers,**
- forming a gate electrode inside the inner sidewall spacers on a cleaned surface of the silicon layer,**
- forming external sidewall spacers adjacent to the inner sidewall spacers, and**
- doping the source/drain regions, [[,]]**
- whereby a recessed channel is formed in the SOI silicon layer between the raised source/drain regions thereabove [[above]] and below the level of the SiGe layer.**

**Claim 12 (currently amended): The method of claim 11 wherein the etch stop layer over the raised source/drain layer comprises silicon oxide.**

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**Claim 13 (currently amended): The method of claim 11 including:**

forming the exterior masking layer [[is]] composed of silicon dioxide which covers the outside spacer layer until after filling the gate electrode space with the gate electrode, [[and]]  
performing planarization of the gate electrode, and  
then stripping the exterior masking layer.

**Claim 14 (original): The method of claim 11 including:**

forming the exterior masking layer of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and after planarization of the gate electrode, and  
then recessing the outside spacer layer down to the etch stop layer adjacent to the gate electrode.

**Claim 15(original): The method of claim 11 wherein the insulator forming the substrate comprises silicon oxide.**

**Claim 16 (currently amended): The method of claim 11 wherein:**

the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer,  
then performing an extension implant to form a raised source extension region and a raised drain extension region, and  
then forming an exterior spacer aside from the gate electrode.

**Claim 17 (currently amended): The method of claim 16 wherein the internal etch stop layer ~~stopping film~~ is stripped away after forming the recess and before performing the extension implant.**

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**Claim 18 (original): The method of claim 17 wherein a halo implant is performed contemporaneously with the extension implant.**

**Claim 19 (original): The method of claim 16 wherein the external sidewall spacers fill the recess.**

**Cancel claim 20 without prejudice.**

**Claim 20 (canceled):**